

REMARKS

Claims 1-20 are pending in the present application.

Applicant respectfully requests reconsideration of the application in view of the remarks appearing below.

Rejection Under 35 U.S.C. § 102

The Examiner has rejected claims 1 through 20 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,636,658 to Arakawa, stating that Arakawa discloses a circuit comprising "a first transistor (C_1)", and "a second transistor (C_2)", all connected and operating similarly as recited by Applicants. The Examiner then asserts that Arakawa expressly states that there is a predetermined ratio between the capacitances C_1 and C_2 , which is established due to the difference between the "gate electrode areas".

Arakawa discloses an alternating current (AC) voltage divider used to create a linear output voltage by means of a capacitor divider. The transfer function $V_{(out)}/V_{(in)}$ is well known for an AC capacitor voltage divider and is quoted in Col. 3, line 35, of the Arakawa patent as $V_M = C_1/(C_1+C_2)*IVP_0$. In this equation, IVP_0 is an applied AC waveform which is shown in Figure 3 of the Arakawa patent. The capacitor divider provides a linear fraction of the changing input voltage IVP_0 on output node V_M . This circuit works by use of classical displacement current through the capacitors and is controlled by $I_c = C dv/dt$.

In contrast, Applicants' claimed invention is a voltage divider for DC voltages. The voltage divider circuit of claim 1 includes transistors, not capacitors, and provides for a specific electrode to source/drain connection between the first and second transistors. Transistors are not capacitors, and so the rejection of the claims in view of Arakawa is necessarily defective under 35 U.S.C. § 102. Further, it is not possible to achieve the recited electrode to source/drain connection called for in claim 1 with capacitors since they lack electrodes, sources and drains in the sense these terms are used in relation to transistors. In addition, the invention of claim 1 requires a relationship in the areas of the gate electrodes of the first and second transistors that cannot be accomplished with a capacitor that lacks gates and hence gate electrodes.

The novelty of the claimed invention is further apparent when the differences in operation between Applicants' voltage divider circuit versus Arakawa's voltage divider circuit are considered. Applicants' invention uses tunneling conduction, not displacement current, to accomplish voltage division using a DC input voltage (VDD). The Arakawa patent is silent with

respect to creation of a voltage divider using tunneling elements. Instead, the Arakawa patent is directed to the division of a time-changing voltage (i.e., AC voltage) to a linear fraction using a standard capacitor voltage divider and specific types of polycrystalline layers. Application of a DC voltage from 0 volts to the Arakawa voltage divider will result in the flow of only a transient current, and a stable and predictable voltage on node N1, presumably a goal of the Arakawa invention, will not be possible.

These differences between the voltage divider circuit of claim 1 and the subject matter of the Arakawa patent also apply to the voltage divider of claims 7 and 16 and the methods of claims 12 and 20. As such, all claims in the present application are believed to be novel over Arakawa.

In view of the preceding comments, it is clear that Applicants' claimed invention is novel over the Arakawa patent. Further, there is no suggestion in the Arakawa patent or elsewhere that the invention described therein could be expanded to cover Applicants' claimed invention.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present anticipation rejection.

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-20 are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

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